



TECHNICAL INFORMATION

LOW INDUCTANCE CAPACITORS FOR DIGITAL CIRCUITS

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Abstract:

Ceramic capacitors have become one of the limiting factors in digital circuits because of intrinsic characteristics such as equivalent series resistance and inductance. There are many things which could be done to mitigate that, and we describe some of those in this paper. AVX's DCAP capacitor, (developed with and for IBM) is used as a benchmark to show how much can be done to improve the situation. We compare and contrast that part to those currently available.

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Introduction

The dramatic increase in speed and packing density of microprocessor and memory chips has required a corresponding advancement in passive components, particularly ceramic decoupling capacitors.

A standard design element used by circuit designers, ceramic dielectrics are very stable with respect to environmental changes, compact, and in form factors which are conducive to most packaging schemes.

The concurrent development of capacitors with the major OEMS has been a driving force to accomplish many design innovations. Until recently, however, some of the advanced designs have been proprietary to those customers, and not generally available. Recently, the “door has been thrown open”, and AVX is able to offer an entire new spectrum of parts to the electronics industry. In this paper, we describe a range of parts which are now, or soon will be, available. The key parameter of concern is inductance, which robs efficiency from circuit designs.

Why low inductance?

In today's high speed digital circuits, the power supply is typically located some distance away from the microprocessor it drives. When the logic switching requires a pulse of energy, it must pull this energy along the entire path length from power supply to the logic device. This creates a variety of design problems. First, there are resistance losses, which rob energy away and dissipate it as heat. Second, and more significant, is the loss due to current changes through the path inductance. This creates a “delta-i” noise pulse and/or a voltage drop which, in turn, can cause logic errors (see the box “ESR and ESL effects ...”). This noise pulse is conducted back to other circuits or radiated out to contaminate its neighbors.

Circuit engineers have attacked this problem in a number of ways: reducing the path length, lowering the inductance, and (our personal favorite), installing a decoupling capacitor close to the logic. These have all worked fine, but as switching speeds increase, more subtle losses can occur that must be eliminated.

As it turns out, yesterday's standard decoupling

capacitor may be a sub-optimal approach to high speed decoupling. The internal resistance and inductance have become major issues.

The capacitor, then and now:

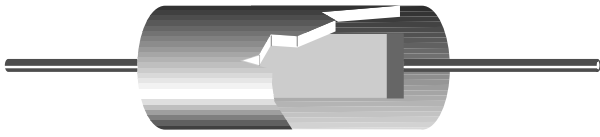
Circuit level decoupling applications

When first developed, ceramic capacitors were encapsulated and leaded. As circuit board designs began to adopt surface mount technologies, the capacitor evolved to a simpler configuration. There were two aspects that facilitated this change. First, the internal element of the leaded capacitor was already the required form factor. Second, the elimination of the leads reduced the intrinsic inductance of the capacitor by at least 33%.

That simple expedient has satisfied circuit designers for a number of years. However, the technological gains utilized in the design and construction of the computer system architecture has out-paced those gains. Operating speeds have increased, voltage and power consumption have decreased and system efficiency has become a more critical design factor. Capacitor performance has to be improved to continue the reduction of the internal inductance. As we will see shortly, considerable progress has been made to keep pace with the demands of today's high speed circuit designs.

Throughout the balance of this paper, we will discuss several generations of MLC capacitor designs that provide decreasing internal inductance values. We will look at each configuration with greater detailed explanations of the new innovative designs. In summary, these products are:

<u>MLC Capacitor</u>	<u>Typical Inductance at .01 pF</u>
Axial Leaded MLC	2000 pH
0805 SMD	1400 pH
0508 SMD	700 pH
KCAP	300 pH
DCAP	50 pH



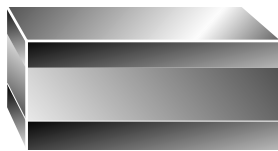
Axial Leaded MLC

The above cross-section shows the AVX Spinguard™ which had been the most popular capacitor for decoupling only a couple years ago. Available in a wide range of sizes, values and TCC's, over 80% of the parts sold were for decoupling. It has an internal inductance of over 2000 pico-henries.



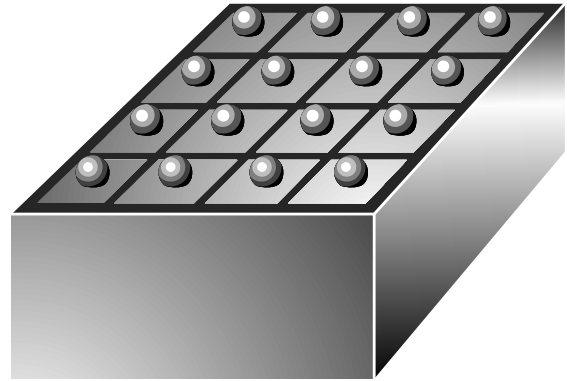
0805 SMD

The next most obvious choice for surface mount conversions was simply to use the internal element for the axial part, with provisions made for easier soldering by the customer. A considerable emphasis was placed on cosmetics, and immunity to a wider range of soldering conditions. A typical example, shown above, is the 0805 capacitor (0.080 in. long x 0.050 in. wide), with an internal inductance of 1400 pico-henries.



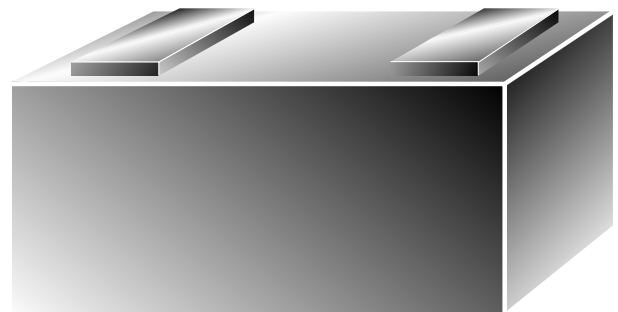
0508 SMD

As inductance became more of a concern, a first order effect could be attained by relatively simple geometric considerations. By altering the aspect ratio of the capacitor, as shown above (e.g. from an 0805 body to an 0508 body), the inductance could be lowered considerably. Together with improved conductivity of the electrodes, the inductance of this design became about 700 pico-henries.



DCAP

We take a giant leap here, with the consideration of the DCAP. In IBM's designs for the ES/9000 module, as documented in several published papers (eg: Davidson et al), the demands for low inductance, and low ESR outlined the need for a major improvement in the decoupling device. After considerable modeling, and joint development activity between IBM and AVX, the result was DCAP. This part has been in production for several years, and has demonstrated its worth by being incorporated into IBM's newest systems. The inductance of this part is typically 50 pico-henries, since it utilizes the thin-film metallization/C4 solder ball technology for flip-chip substrate attachment. Platinum electrodes are employed to lower ESR and to provide inertness to reducing atmospheres. In the production of this part, manufacturing tolerances are held to <0.001 in. (for more details, see the "DCAP Design" section below.)



LICA

In many cases, it may not be necessary or cost effective to use the complete DCAP system. For such instances, we have been developing an array of unique custom parts for some customers, which are, typically application specific designs. In general, however, we can speak of that range using a generic form we call "LICA", Low Inductance Capacitor Arrays. It is not a single part, but a range of parts which take advantage of some of the low inductance design technologies we learned on DCAP and elsewhere.

The range of improvements can come from:

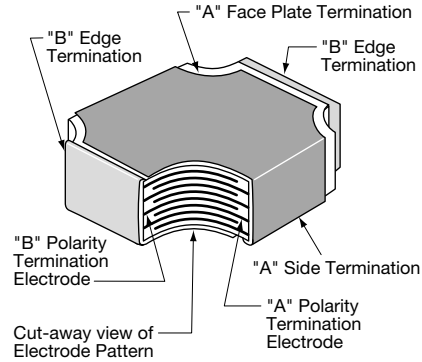
- low aspect ratio
- low ESR electrode/termination system
- perpendicular electrodes (to the circuit)
- inter-digitated tabs, multiple pickups
- thin-film surface circuitry (for close proximity)
- C4 mounting systems

By employing some or all of these improvements, we can develop what is effectively an application-specific approach to satisfying a broad range of low inductance requirements. Because of our expertise in flip-chip compatible, thin film metallization technologies, these devices are ideally suited for Multi-Chip Module (MCM) applications.

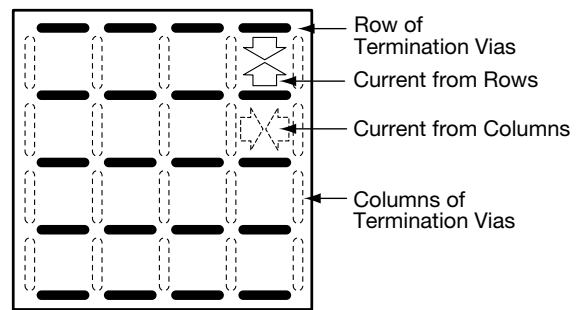
Board-level applications and others

At the power supply end of the system, the needs are still present for lowered inductance, but now with much greater capacitances, on the order of Microfarads, instead of the Nano-farads discussed above and later.

Here, some of the same answers apply, but the relief of size constraints allows more flexibility. Our Advanced Products Group has developed some low inductance configurations that are unique, and efficient. The sketches below show some configurations which are used.

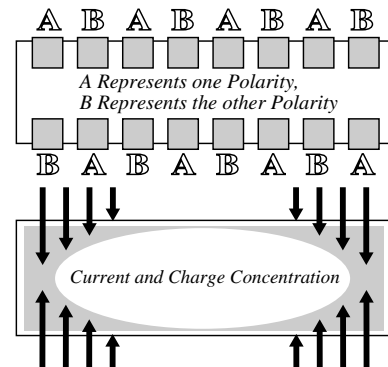


The "Power Plane Decoupling Capacitor" has a four terminal construction to generate inductance canceling. This 1-4 micro-farad device has inductances of about 100 pico-henries. Each face has a conductive surface to connect common electrodes.



Terminations are full face. All Rows common to one face and all columns common to opposite.

When the capacitance gets higher, on the order of 10 microfarads, the capacitor becomes too large for cancellation effects, but it can be broken up into segments, each of which meets the cancellation criteria. The capacitor depicted here is a 10 MF capacitor whose self-resonance is 13 Megahertz, which translates to an ESL of 15 picohenries!



The DIP configuration can allow unique cancellation advantages using the concept of "interdigitation". Here we see a drawing of that. The ideal format for this device would be circular, as it would permit absolutely uniform charge concentration.

The DCAP design and parameters

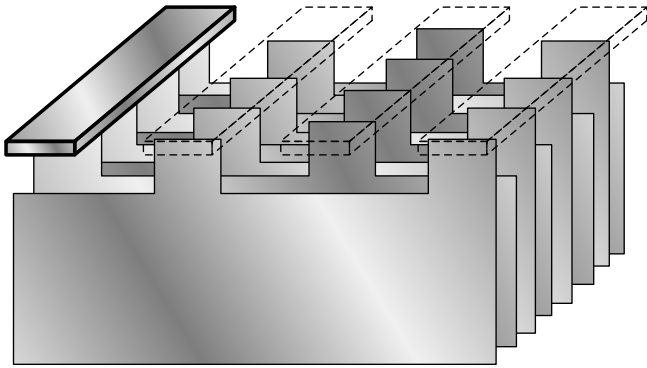


Figure 1: Representation of electrode/tabs on DCAP

The current DCAP design is depicted in Figure 1. This drawing has been simplified to depict the key design features. The actual product part has four separate capacitor sections, and each section has eight electrode sets. The electrodes each have two tabs spaced so that there is redundant pick-up, and each set of tabs is mated with a surface metallization strip, to which “C4” solder balls are bonded. The capacitor is built so that the tabs exit what is normally considered the side of the part. The capacitor body dimensions are nominally 0.063 x 0.073 x 0.035 inches (1.6 x 1.85 x 0.875 mm). Each tab has one solder ball, about 5 mils in diameter. The schematic is shown in Figure 2.

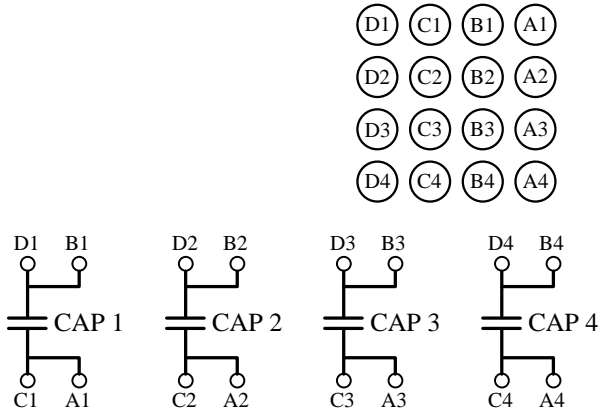


Figure 2: Equivalent Circuit and Pin-outs for DCAP

Since most electrical circuits operate above room temperature, the convention of designing parts to 25°C was abandoned, and the typical temperature of 55°C was chosen. The ceramic was modified to have its optimum properties under those conditions, rather than the almost arbitrary conditions of typical incoming inspection. Figure 3 displays the Temperature Coefficient (TCC) for the standard DCAP.

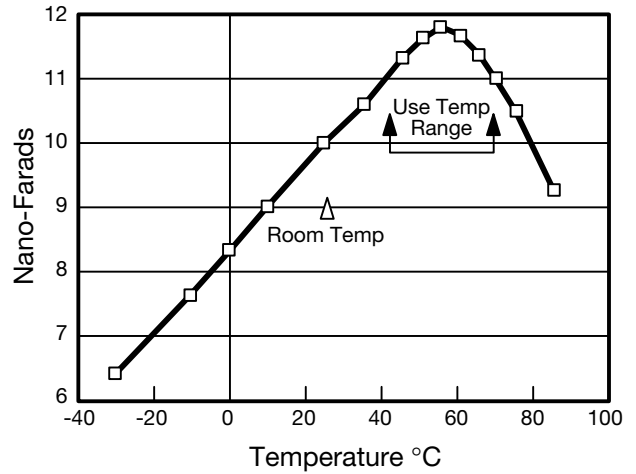


Figure 3: Capacitance versus Temperature for the DCAP

This particular ceramic is also resistant to high-temperature reducing atmospheres. Each of the four capacitors in the array has the following parameters:

- Capacitance at 25°C:.....8 nF
- Capacitance at 55°C:.....10 nF
- Dissipation Factor, 25°C:.....5 %
- Dissipation Factor, 55°C:.....3 %
- Max DF at 500 MHz:40 %
- Inductance (Typ):.....45-60 pico-henries
- DC Resistance:(Typ)70 milli-ohms
- DC Leakage, 10V:(Typ)<2 nano-amps
- Insulation Resistance:.....>50 Giga-ohms
- Use Frequency, to:1 Giga-Hertz
- Dielectric Withstanding:.....1000 Volt minimum
- Rated Voltage:50 volts DC

The Future

As the devices get smaller and smaller, there comes a point where separate capacitive components no longer makes sense. Our current MLC line for surface mount product extends down to an "0402" size (40 mils by 20 mils). In addition to the obvious difficulty of handling that size part, the overhead for insulative margins on the side and the ends becomes comparatively larger, and volumetric efficiency drops off drastically. Most are now predicting that the next generation will require decoupling solutions as part of the ceramic package. AVX is working with Kyocera to develop those schemes. Several of the leading IC manufacturers have expressed more than a passing interest in these products for the late 90's.

Summary

The role of the capacitor in future digital designs will continue, but their specific operating characteristics must progress in order to support the overall system requirements without resistive or inductive contributions. Form factors must change to permit more compact packaging and reduction of path lengths. Internal inductance improvement will be necessary, but will probably be determined as much by cost constraints as circuit optimization.

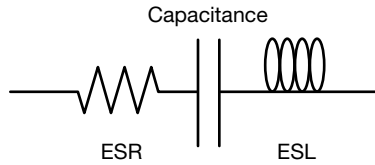
By making available of the DCAP capacitor, a new benchmark has been set for very low inductance. With the two ends firmly established, a range of devices can be built to satisfy almost any requirement efficiently.

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ESR and ESL Effects on Logic

Equivalent Capacitor Circuit

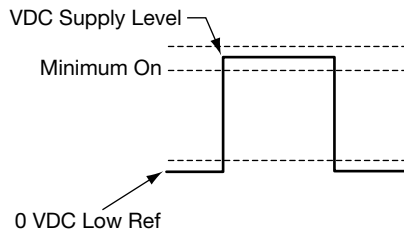


The capacitor is not just a capacitor. It contains parasitic elements to rob its performance.

ESR or effective series resistance is the power loss element. It is resistive in that as energy passes through, some portion is converted to heat and lost.

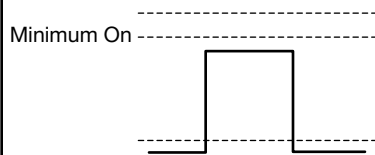
ESL or effective series inductance is a figure associated with a magnetic field buildup as current moves through the device. It causes the current to delay reaching its peak, and then it causes the current to continue increasing after the input peak has been reached.

Logic Requirements



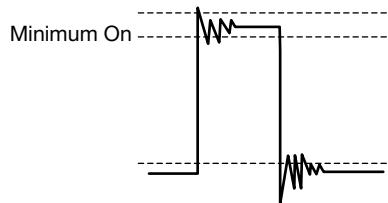
Logic circuits operate within one of two states: on or off, high or low, true or false... The determination or read of any elements state is its measurement of voltage level. The determination is not equally divided as greater than half on or less than half on. It is a defined level near the nominal voltage of the supply. There is a window of acceptability where the logic state is properly read 100% of the time. Then there is that indeterminate state where it nears the minimum level of acceptability.

Power Droop Effects



When the IC demands many power bursts and the delay to refresh the local decoupling capacitor is excessive, droop occurs. This might also occur on a board level if all the ICs demand refresh power at once. The energy transfers throughout the entire decoupling scheme must allow for worst case scenarios and still function without error. This condition is prevalent when the total capacitance is lacking.

High Frequency Noise



Every time energy is taken from a capacitor, it screams. Get enough screaming at one time and-glitch, pop, crash! Even if one capacitor generates this scream, if its loud enough, the results may be the same.

The scream is a voltage pulse generated mostly by the parasitic inductive element in the decoupling circuit. It may occur at only the setting of the state for one group of elements and die out before the read occurs, but it may occur during the read of another groups' state.

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